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1 ~~151~~. (Amended) A method of controlling a memory device by a
2 memory controller, wherein the memory device includes a plurality of
3 memory cells, the method of controlling the memory device
4 comprises:

5 providing first block size information to the memory device,

6 ~~151~~ wherein the first block size information is provided by the memory
7 controller and is representative of a first amount of data to be input
8 by the memory device; and

9 issuing a first operation code to the memory device, wherein in
10 response to the first operation code, the memory device inputs the
11 first amount of data.

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1 ~~152~~. The method of claim ~~151~~ wherein the memory device inputs the
2 first amount of data synchronously with respect to an external clock
3 signal.

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1 ~~153~~. (Amended) The method of claim ~~151~~ further including:
2 providing second block size information to the memory device,
3 wherein the second block size information defines a second amount of
4 data to be input by the memory device; and

5 issuing a second operation code to the memory device, wherein in
6 response to the second operation code, the memory device inputs the
7 second amount of data.

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1 ~~154~~. (Amended) The method of claim ~~151~~ wherein the first block
2 size information and the first operation code are included in a request
3 packet.

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1 ~~155~~. (Amended) The method of claim ~~154~~ wherein the first block
2 size information and the first operation code are included in the same
3 request packet.

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1 ~~156~~⁶. (Amended) The method of claim ~~151~~¹ further including providing
2 the first amount of data to the memory device.

1 ~~157~~⁷. (Amended) The method of claim ~~156~~⁶ wherein the first amount
2 of data is provided to the memory device after a delay time transpires.

1 ~~158~~⁸. (Amended) The method of claim ~~157~~⁷ wherein the delay time is
2 representative of a number of clock cycles of an external clock signal.

1 ~~159~~⁹. (Amended) The method of claim ~~151~~¹ wherein the first block
2 size information is a binary representation of the first amount of
3 data.

1 ~~160~~¹⁰. (Amended) The method of claim ~~151~~¹ wherein the first amount
2 of data is output, by the memory controller, synchronously with respect
3 to an external clock signal and during a plurality of clock cycles of
4 the external clock signal.

1 ~~161~~¹⁴. (Amended) A method of operation in a synchronous memory
2 device, wherein the memory device includes a plurality of memory cells,
3 the method of operation of the memory device comprises:

4 receiving first block size information from a memory controller,

5 wherein the first block size information represents a first amount of
6 data to be input by the memory device in response to an operation code;

7 receiving the operation code, from the memory controller,
8 synchronously with respect to an external clock signal; and

9 inputting the first amount of data in response to the operation
10 code.

1 ~~162~~¹⁵. (Amended) The method of claim ~~161~~¹⁴ wherein inputting the first
2 amount of data includes receiving the first amount of data
3 synchronously with respect to the external clock signal.

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1 ~~163~~. (Amended) The method of claim ~~162~~ wherein the first amount
2 of data is sampled over a plurality of clock cycles of the external
3 clock signal.

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1 ~~164~~. (Amended) The method of claim ~~161~~ wherein the first block
2 size information and the operation code are included in a request
3 packet.

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1 ~~165~~. (Amended) The method of claim ~~164~~ wherein the first block
2 size information and the operation code are included in the same
3 request packet.

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1 ~~166~~. (Amended) The method of claim ~~161~~ wherein the first block
2 size information is a binary representation of the first amount of data
3 to be input in response to the operation code.

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1 ~~167~~. (Amended) The method of claim ~~161~~ wherein the first amount
2 of data is output, by the memory controller, synchronously during a
3 plurality of clock cycles of the external clock signal.

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1 ~~168~~. (Amended) The method of claim ~~161~~ further including
2 generating an internal clock signal, using a delay locked loop and the
3 external clock signal wherein the first amount of data is input
4 synchronously with respect to the internal clock signal.

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1 ~~169~~. (Amended) The method of claim ~~161~~ further including
2 generating first and second internal clock signals using clock
3 generation circuitry and the external clock signal, wherein the first
4 amount of data is input synchronously with respect to the first and
5 second internal clock signals.

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~~170~~ 32 The method of claim ~~169~~ wherein the first and second internal
2 clock signals are generated by a delay lock loop.

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~~171~~ (Amended) A method of operation of an integrated circuit,
2 wherein the integrated circuit includes a dynamic random access memory
3 array having a plurality of memory cells, the method of operation
4 comprises:

5 ^{ans 33} > receiving block size information from a controller, wherein the
6 block size information represents an amount of data to be input in
7 response to an operation code;

8 receiving the operation code from the controller; and
9 inputting the amount of data in response to the operation
10 code.

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~~172~~ 29 (Amended) The method of claim ~~171~~ further including storing
2 the amount of data in the memory array.

1 ³¹
~~173~~ 29 (Amended) The method of claim ~~171~~ wherein the block size
2 information and the operation code are included in a request
3 packet.

1 ³²
~~174~~ 29 (Amended) The method of claim ~~171~~ wherein the block size
2 information is a binary representation of the amount of data to be
3 input in response to the operation code.

1 ³³
~~175~~ 29 (Amended) The method of claim ~~171~~ wherein the amount of data
2 is input, in response to the operation code, after a delay time
3 transpires.

1 ³⁴
~~176~~ 33 The method of claim ~~176~~ wherein the delay time is
2 representative of a number of clock cycles of the external clock
3 signal.

Kindly ADD the following claims:

1 ¹⁶~~178~~. (New) The method of claim ⁴~~151~~ wherein the first operation
2 code is issued onto a bus.

1 ¹³~~179~~. (New) The method of claim ^{11/1}~~178~~ wherein the bus includes a
2 plurality of signal lines to multiplex control information, address
3 information and data.

1 ¹³~~180~~. (New) The method of claim ¹~~151~~ further including providing
2 address information to the memory device.

1 ²⁴~~181~~. (New) The method of claim ¹⁴~~161~~ wherein the operation code, the
2 first block size information and address information are included in a
3 packet.

1 ²⁵~~182~~. (New) The method of claim ¹⁴~~161~~ further including receiving
2 address information from the memory controller.

1 ²⁶~~183~~. (New) The method of claim ¹⁴~~161~~ wherein the first block size
2 information, and the operation code are received from an external bus.

1 ²⁷~~184~~. (New) The method of claim ²⁶~~183~~ wherein the first block size
2 information, and the operation code are received from the same external
3 bus.

1 ²⁸~~185~~. (New) The method of claim ²⁷~~184~~ wherein the external bus is
2 used to multiplex address information, control information and
3 data.

1 ³⁵~~186~~. (New) The method of claim ²⁹~~171~~ further including receiving
2 address information from the controller.